ISTFA 2015 Abstract

X-Ray Microscopy and Root Cause Analysis in Electronic Packaging

L. Mirkarimi, A. Gu, L. Hunter and R. Estrada
Carl Zeiss X-Ray Microscopy, 4385 Hopyard Road, Suite 100 Pleasanton, CA 94588

G. Guevara, M. Huynh and R. Katkar
Invensas Corporation, 3025 Orchard Pkwy, San Jose, CA 95134

Qualification of electronic package technologies requires electrical testing at standard JEDEC environmental test conditions. Finding an electrical failure through electrical test is straight forward; however, determining the root cause of the failure is generally much more difficult. Routine electronic packaging failure analysis utilizes a work flow with a minimum of 8 steps including electrical test, 2D X-ray alignment of part to a dicing saw, dicing the package, mechanical polishing, ion milling, metal sputter coating, scanning electron microscopy imaging and root cause analysis. This traditional process provides two dimensional images of defects from the sample of interest. In this paper we describe an alternative failure analysis workflow involving X-ray microscopy, which effectively reduces the total number of analysis steps. Due to the non-destructive nature of X-ray, both 3 dimensional images of defects as well as 2 dimensional cross sections are effectively used to analyze true root cause of failures.

We have selected several case studies for this paper. The first is a package on package application, where the bond via array (BVA) technology is used. Since it is critical to meet the JEDEC standard, the package made by the new technology must be stressed until first failures. This helps to predict what failure modes are possible with these emerging package technologies. The 14x14mm package on package parts were tested to the JEDEC standard JESD22-A104D board level temperature cycling. First failures were observed in excess of 1700 cycles, well above the requirement. The initial failures were found as a x percent increase in resistance. Cross sectional analysis of the solder interconnect is shown in Figure 1. The crack in the solder interconnect is at the edge of the interconnect and appears to be a standard fatigue crack. While the evidence in the image seemed clear, there were two concerns we had before drawing a final conclusion from this image.

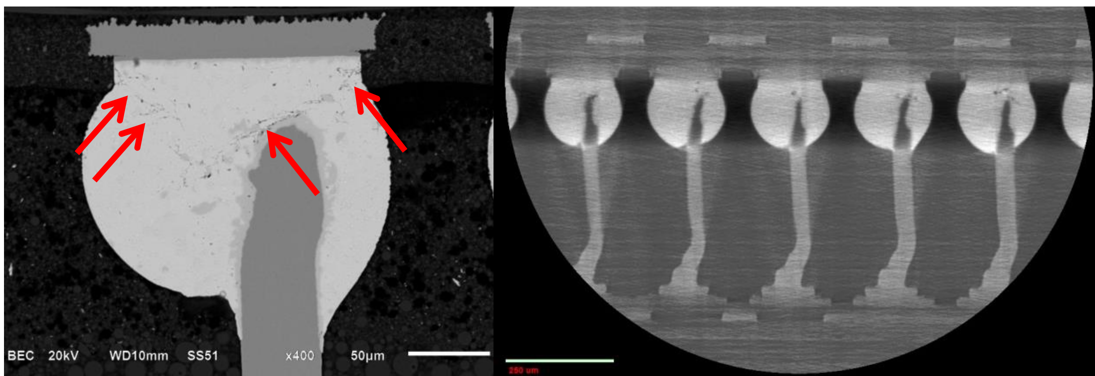

Figure 1(a): Cross Sectional SEM Image of high resistance interconnect. (b) XRM Image of multiple resistance interconnect.

Pure metal systems mixed with solder are prone to electro-migration defects and kirkendal voids near the interface of solder and metal. Additionally, we know from careful characterization of the BVA joints that there is an intermetallic compound at the interface of the Cu wire and at the substrate Cu pad. Intermetallic compounds are brittle and tend to be sources of crack initiation; questioning the true root cause analysis.

Therefore, we scanned additional packages on the same board that did not show increased electrical resistance with a Versa 510 X-ray microscope (XRM) to obtain three dimensional images of the many interconnects on the remaining packages. The virtual cross sections of these parts are shown in Figure 2. In these images all of the voiding and or cracking is occurring at the tip of the wire and solder joint interface. This definitively shows that the early stages of voiding and or cracks within the solder occur near the tip of the wires. Therefore, the original SEM image (Figure 1) with cracks across the entire interconnect at the edge of the joint were not able to explain the whole story. In fact, the strength of XRM is that we can survey many interconnects non-destructively throughout the environmental stress conditions and visualize crack propagation. Preserving the part without disturbing the crack is immensely valuable. With the XRM technique, we image and analyze the defects in the local environment and the failure mode is preserved. In contrast, SEM imaging requires physical cross-section which may alter the defective areas. Mechanically stressing a package can lead to further growth of already existing cracks. Therefore, we have moved to the XRM method, where we screen samples throughout the cycles, enabling us to visualize possible early failures and track them over the cycles. Additional images showing the three dimensional voided areas around the tip will be discussed in detail.

In the second case study the package is a flip chip package with a (40mm by 40mm) footprint. The package was assembled and the electrical test indicated that the package was fine. However, x-ray inspection showed that there were fatigue joint cracks after a single reflow due to the stress in the package. The full three dimensional images of the cracks in the interconnects in the case studies described above will be discussed in more detail. The full XRM study allows the volume calculation of voids and cracks in the interconnect, which may be useful to validate fundamental crack propagation models.

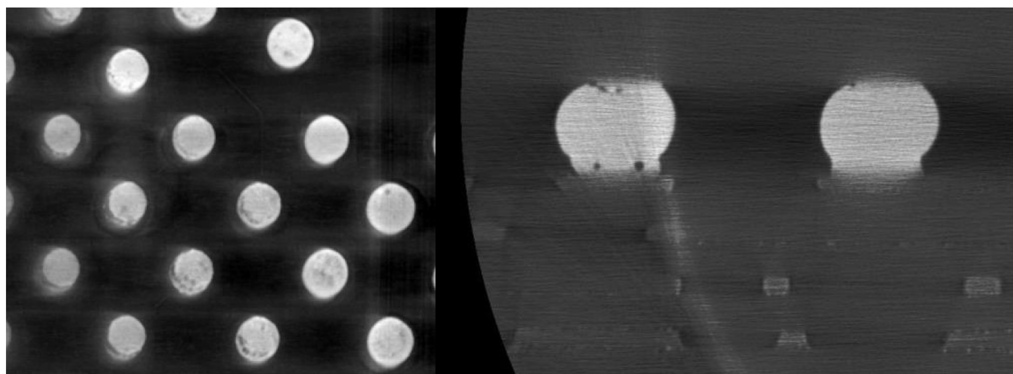

Figure 2 (a) Top View of 3D X-ray images and, b) virtual cross-section of the interconnects