Accelerate the Development of Advanced IC Packages Using 3D X-ray Microscopes to Measure and Characterize Buried Features

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Reduction in product development cycle time and improvements in early product manufacturing yields are strategic objectives for many technology-driven firms. At the same time, product complexity is increasing, especially in areas such as IC packaging where the DRAM “wall” and the slowdown in Moore’s law are pushing product performance improvements from the silicon and into the IC package. These goals may conflict, however, and firms might be forced to consider trade-offs between product performance and packaging yields.

As shown in Figure 1, for nearly 40 years the IC packaging industry has relied extensively on physical cross-sectioning to view and measure buried interconnects. New technologies such as 3D X-ray microscopes are needed to provide submicron-resolution, semi-automated measurement of buried interconnects in advanced packages. These solutions will help to enable faster time to market by reducing learning cycles through delivery of richer, higher-accuracy engineering data compared to traditional destructive methods.

**Acceleration of Package Interconnect Scaling**

Dennard Scaling and Moore’s Law drove performance improvements in the semiconductor industry for nearly 50 years. In this environment it was often more beneficial to scale features in the silicon than to scale features in the IC package. As a result, package technologies tended to focus on feature sizes that could be manufactured without sophisticated process controls.

However, Dennard Scaling peaked in the early 2000s and Moore’s Law has slowed to the point where nearly all leading electronics companies are searching for advanced package-level solutions to improve product performance. These advanced package-level solutions are pushing packages out of their traditional comfort zones and into technologies which require advanced closed-loop process controls. As shown in Figure 2, the minimum practical flip chip pitch was considered to be around 150 µm when IBM began to commercialize C4 flip chip BGA technology in the 1980s. A 150 µm pitch C4 flip chip results in a maximum interconnect density of around 50 I/O per mm² and can be assembled with relatively high-yields without complex process controls. In the early 2000s Cu-pillar flip chip was first commercialized; use of Cu-pillar enabled significantly finer interconnect pitch than C4 flip chip because the solder fillet shape was easier to control. A 100 µm-pitch Cu-pillar flip chip has a maximum interconnect density of 100 I/O per mm² and can also be assembled with relatively high-yields without complex process controls.

High Bandwidth Memory (HBM) and Hybrid Memory Cube (HMC) pioneered the mass-production of high-density 50 µm pitch Cu micro-pillar interconnects. These micro-pillars feature an interconnect density of 400 I/O per mm² and require more sophisticated process controls to maintain acceptable yields. Going forward, future generations of advanced memory integration and logic “disaggregation” technologies such as chiplets will drive flip chip interconnect pitch down to 40 µm, 30 µm, 20 µm and even 10 µm! As the interconnect pitch approaches and scales below 40 µm the following changes are expected:

- The solder cap will become smaller and will evolve into a thin solder coating
- The solder coating on the Cu-pillar will eventually be replaced by Cu-to-Cu diffusion bonding

**Figure 1. Optical inspection circa 1970.**
*Courtesy Intel Museum Archives*

**Figure 2. Flip chip interconnect roadmap from C4 solder to direct Cu (150 µm to 10 µm).**
At all levels of pitch evolution, process characterization and process controls will become more and more critical, and will exceed the capabilities of existing package engineering inspection and measurement systems.

**Comprehensive Process Control Systems in Wafer Fabs**

In the late 1980s wafer fabs began to deploy sophisticated optical inspection and closed-loop process control systems[1]. These control systems were vital to realizing the performance improvements predicted by Dennard Scaling and Moore’s Law, while at the same time accelerating yield learning (e.g. the speed of improving yield) ultimately speeding-up time to market. Unfortunately, advanced package assembly often relies on bumped interconnects and the optical systems developed for wafer fabs are not usable with these “buried” interconnects. New, advanced inspection and measurement technologies are needed to achieve accelerated yield learning for advanced IC packages as there is a lot at stake.

**The Cost of a Packaging Delay**

Delays in solving package development problems can result in missed product shipments. While numerous scenarios have been developed for calculating the cost of a product delay, we are going to use a simple model here which assumes that a delayed IC package results in a first-year loss-in-revenue which is proportionate to the length of the delay. As shown in Table 1, the cost of a one-quarter packaging delay for a product would be 25% of the first-year revenue, or $2.5M in the case of a product with $10M in first-year revenue.

**Table 1. Cost of packaging delay.**

<table>
<thead>
<tr>
<th>1st Year Product Revenue</th>
<th>Lost Revenue Due to 1 Quarter Delay</th>
</tr>
</thead>
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<tr>
<td>$10M</td>
<td>$2.50M</td>
</tr>
<tr>
<td>$50M</td>
<td>$12.5M</td>
</tr>
<tr>
<td>$100M</td>
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**X-ray Microscope: Leading Technology for High-resolution, Non-destructive Package Analysis**

For nearly a decade the X-ray Microscope (XRM) has been the leading technology for high-resolution, non-destructive analysis of buried defects in IC packages[4]. XRM imaging is often used in the failure analysis workflow to image suspected locations of electrical failures prior to physical failure analysis. Figure 3 shows examples of the wide range of package defects that can be imaged by an XRM. Because an XRM can provide advanced knowledge of the physical characteristics of the failure, such as size and orientation, it helps improve the success rate of physical failure analysis thereby improving the chance of successfully determining the root cause of the failure. It is for this reason that nearly every failure analysis lab in the world for advanced packages uses an XRM.

X-ray microscopes are often chosen over microCT-based X-ray systems because XRM do not lose resolution as package body size increases, as shown in Figure 4. For both microCT and XRM systems, the process of generating 3D images is accomplished through computed tomography, which requires samples to rotate at least 180°. Since samples are rotated, they must be moved far-enough away from the source to avoid colliding with it. This increase in distance has an adverse impact on microCT-based systems because resolution degrades as the sample moves away from the source; XRM systems use optics to compensate for the increase in distance and thus do not lose image resolution.

**Inspection and Measurement of Buried Features in Advanced IC Packages**

Carl Zeiss SMT, Inc. has developed an inspection and measurement system for buried features in advanced IC packages using the proven ZEISS Xradia 620 Versa X-ray microscope. This system, called RepScan, extends the application of the Versa XRM into the areas of...
The RepScan system includes a patented Automatic Tomography Acquisition system that enables automated loading, scanning and unloading of identical samples without the need for operator intervention. Scan results may be automatically transferred to a separate workstation where a variety of measurements may be executed semi-automatically. This establishes a new benchmark for non-destructive measurements that support process optimization, product development and QA/QC of complex fine-pitch 3D architectures, including 2.5D interposers, high bandwidth memory stacks with TSVs and microbumps, wafer-level packages with package-on-package interconnects and ultra-thin memory with multiple chips in a stack.

Versa RepScan Case Studies
As shown in Figure 6, RepScan addresses many of the limitations of physical cross-sectioning and offers new capabilities:

- Enables statistically-valid sample quantities with semi-automated, highly repeatable linear as well as volumetric measurements
- Improves the ability to detect anomalies because samples can be imaged and measured in any direction
- Allows for further testing of samples after analysis because the RepScan methodology is non-destructive

Below are three sample case studies which demonstrate the capabilities of Versa RepScan measurement:

- Flip Chip Bond Line Thickness
- Flip Chip Solder Fillet Extrusion
- Flip Chip Solder Bump Wetting

Case Study #1:
Flip Chip Bond Line Thickness
Flip chip bond line thickness is one of the most important factors to be considered when designing a bumped joint, as there are electrical, mechanical, thermal as well as underfill considerations. Bond line thickness is generally not uniform across the die due to factors such as warpage and tilt. In addition, as geometries decrease and as processes migrate from mass-reflow to thermo-compression bond, measurement and control of bond line thickness becomes even more critical.

As shown in Figure 7, the 3D X-ray dataset was used to identify the boundary between the solder and the Cu pad/pillar. 3D X-ray images can effectively determine the exact location of this boundary using material segmentation (i.e., the transition from Cu pad/pillar to Sn-based solder).

Case Study #2:
Flip Chip Solder Fillet Extrusion
Solder fillet shape in mass reflow is determined by a number of factors including solder volume, pad size, solder wetting, component mass, etc. Ultimately...
shape is determined in all directions on a 2D plane, not just a single direction based on a cross-sectional cut. By comparing the ratio of the solder fillet area to the pad area, we can assess and measure small variations in the bonded interconnect system.

Case Study #3: Flip Chip Solder Bump Wetting

Soldering is a complex chemical process which enables the creation of reliable, low-resistance electrical interconnects between mechanical structures at relatively low (~250°C) temperatures. Good solder wetting is vital to electronics system performance and to reliability; however, wetting itself is difficult to measure. Solder wetting on leaded components can be assessed by the meniscograph (wetting balance) method, but this technique is highly subjective and is not appropriate for small surface-mounted interconnects such as flip chip bumps. As a result, flip chip technology often relies on destructive approaches such as die-shear to indirectly assess the quality of solder wetting.

As shown in Figure 9 (Cu-pillar bump-on-trace), the 3D X-ray dataset was used to calculate the area of the interfaces between the solder and the Cu pad/pillars. As previously mentioned, 3D X-ray imaging is effective at determining the exact location of this boundary because the transition from Cu pad/pillar to Sn-based solder can be detected by the system. Using proprietary algorithms, the areas of these interfaces were compared and used to assess the quality of the solder wetting.

Summary

The use of Versa RepScan enables the extraction of richer statistical data from engineering builds which would have been lost if traditional methods such as mechanical cross-sectioning were used, as shown in Figure 10. Better data extraction results in more accurate statistical analysis and enhanced ability to detect low-level defects, as compared with traditional mechanical cross-sectioning. As a result, products can be developed and launched faster, with fewer cycles of learning and with higher, more stable assembly yields.

References
